REMARKS/ARGUMENTS

Brief Summary of Status

Claims 1-76 are pending in the application.

Claims 45-62, 75, and 76 are allowed.

Claims 1, 2, 5, 6, 11, 14,-16, 18, 19, 21, 22, 26, 29-34, 39-41, 43, 44, 63, 70, 71, 73, and 74 are rejected.

Claims 3, 4, 7, 8, 9, 10, 12, 13, 17, 20, 23, 24, 2, 27, 28, 35, 36, 37, 38, 42, 65, 66, 67, 68, 69, and 72 are objected to.

1. In the above-referenced OA, the Examiner has objected to the specification because of informalities.

2. In the above-referenced OA, the Examiner has rejected claims 1-2, 5, 6, 11, 14, 15, 16, 18, 19, 21, 22, 26, 29, 30, 31, 32, 33, 34, 39, 40, 41, 43, 44, 63, 64, 70-71, 73-74 under 35 U.S.C. § 103(a) as being unpatentable over Umermura, et al. (U.S. Patent No. 6,088,829) (hereinafter referred to as "Umemura") in view of Voit (U.S. Patent No. 6,510,473) (hereinafter referred to as "Voit").

5. In the above-referenced OA, the Examiner has indicated that claims 45-50, 51-62, and 75-76 are allowed.

6. In the above-referenced OA, the Examiner has indicated that claims 45-50, 51-62, and 75-76 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 U.S.C. § 103 (a)

2. In the above-referenced OA, the Examiner has rejected claims 1-2, 5, 6, 11, 14, 15, 16, 18, 19, 21, 22, 26, 29, 30, 31, 32, 33, 34, 39, 40, 41, 43, 44, 63, 64, 70-71, 73-74 under 35 U.S.C. § 103(a) as being unpatentable over Umermura in view of Voit.

In the above-referenced OA, the Examiner states:

"Regarding claims 1, 6, Umemura et al disclose an inter-device adaptable clock skewing system, comprising: a first device (401); and a second device (400) is communicatively coupled to the first device; and wherein the first device comprises a clock generation circuit (an oscillation unit for generating clock signal, col. 3, lines 40-45) for selecting and providing a clock signal to the second device, the clock signal

having a frequency and a phase (col. 3, lines 40 to col. 4, line 26)." (see OA, Part of Paper No./Mail Date 20050427, p. 3).

The Applicant respectfully traverses.

The term "oscillation unit," as identified by the Examiner, only appears 4 times in Umemura, and all of the appearances are in the "SUMMARY OF THE INVENTION" portion as identified below.

"A first aspect of the present invention incarnated in the preferred embodiments thereof as described hereinafter provides a synchronous data transfer system which includes an oscillation unit for generating a clock signal for a predetermined transfer cycle for data transfer, and a plurality of nodes connected to the oscillation unit." (See Umemura, col. 1, lines 57-62, emphasis added).

"A second aspect of the invention is seen in a synchronous data transfer system which includes an oscillation unit for generating a clock signal for a predetermined transfer cycle for data transfer, a plurality of nodes connected to said oscillation unit ... ." (See Umemura, col. 3, lines 40-62).

Also, in the "ABSTRACT", there is mention of an "oscillation circuit".

"A synchronous data transfer system includes an oscillation circuit and a plurality of nodes connected to the oscillation circuit and each including at least an internal logic circuit." (See Umemura, ABSTRACT, lines 1-3, emphasis added).

From this, it appears that the each of the "plurality of nodes" that includes "at least an internal logic circuit" is communicatively coupled to the "oscillation unit." Therefore, the "oscillation unit" if a first device and any node of the "plurality of nodes" (which includes "at least an internal logic circuit") is a second device.

Since the only reference to this "oscillation unit" or "oscillation circuit" in Umemura occurs in the "SUMMARY OF THE INVENTION" portion and the "ABSTRACT" portion, there are no reference numerals provided as to what this actual item (or device) corresponds in the diagrams and "DESCRIPTION OF THE PREFERRED EMBODIMENTS" portion of Umemura.

The only item in any of the diagrams of Umemura that the Applicant can identify as being an "oscillation unit" or equivalent (as asserted by the Examiner in the OA), such that there is a "plurality of nodes connected to the oscillation unit" is the "source

oscillator 100" depicted in FIG. 1. In fact, the only time the term "oscillator" is used in Umemura, it is used in the phrase "source oscillator 100".

As such, the Applicant believes to be correct in correlating the Examiner-cited "an oscillation unit for generating clock signal, col. 3, lines 40-45" portion of Umemura which describes an "oscillation unit" (i.e., within the "SUMMARY OF THE INVENTION" portion) to correspond to the "source oscillator 100" of the "DESCRIPTION OF THE PREFERRED EMBODIMENTS" portion and the diagrams of Umemura.

The "source oscillator 100" provides a "reference clock signal 200" to a number of different nodes (See FIG. 1 of Umemura).

It is noted that this "source oscillator 100" is not implemented within the either of the "first semiconductor chip 401" (i.e., first device) or the the "second semiconductor chip 400" (i.e., second device) which the Examiner identifies in the OA. In other word, neither of the "first semiconductor chip 401" (i.e., first device) or the the "second semiconductor chip 400" (i.e., second device) of Umemura comprises the "source oscillator 100".

"Referring to the figure, the reference clock 200 is supplied from the source oscillator 100 to the semiconductor chips 101a, 101b and 101c, respectively, wherein the phase of the reference clock 200 is referenced in each of the semiconductor chips 101a, 101b and 101c for aligning or matching the phase of the clock signals in the semiconductor chips 101a, 101b and 101c." (See Umemura, col. 19, lines 45-51).

From this, the Applicant respectfully believes that it is appropriate to identify the "source oscillator 100" as being a first device and any one of the "semiconductor chips 101a, 101b and 101c" to be a second device when interpreting the Examiner's assessment of Umemura with respect to the Examiner's reference to the "oscillation unit for generating the clock signal, col. 3, lines 40-45".

It does not appear even capable to perform any selection of the frequency and phase of the "reference clock 200" provided by the first device, or "source oscillator 100", of Umemura. When considering the diagrams of Umemura, the "source oscillator 100" appears to be a crystal type oscillator (See FIG. 1 of Umemura). It is generally known in the art that such crystal type oscillators oscillate at a singular particular

frequency. In the art, absent some indication otherwise, a crystal type oscillator typically simply has a resonant frequency and any "reference clock 200" generated from it simply has the same frequency as the resonant frequency of the crystal type oscillator. At least in Umemura, there is no indication of any ability to select a frequency of this crystal type oscillator.

The first device, "source oscillator 100", or crystal type oscillator of Umemura simply does not provide the limitation of the subject matter as claimed by the Applicant in claim 1 of "wherein the first device comprises a clock generation circuitry, the clock generation circuitry being operable to select and to provide a clock signal to the second device, the clock signal having a frequency and a phase." The first device, "source oscillator 100", or crystal type oscillator of Umemura does not include any "clock generation circuitry being operable to select and to provide a clock signal to the second device", in that, there is no capability to select any frequency from the crystal type oscillator.

Moreover, at least one limitation of the subject matter claimed by the Applicant in claim 1 includes "the first device further comprises a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device."

In the above-referenced OA, the Examiner states:

"Umemura et al fail to disclose the first device further comprising a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device.

Voit discloses a selection control pin (120) in a clock circuit (100) used to select at least one of the frequency of the clock signal and the phase of the clock signal (col. 4, line 54 to col. 5, line 10). It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the of the frequency and phase of the clock signal as taught by Voit into the teaching of Umemura et al for providing a desired clock frequency to the second device." (see OA, Part of Paper No./Mail Date 20050427, p. 3).

The Applicant respectfully traverses.

It would go against the teaching of Umemura to select "the reference clock 200 is supplied from the source oscillator 100 to the semiconductor chips 101a, 101b and 101c".

In contradistinction, it is not the first device, or "source oscillator 100", of Umemura that performs any selection of the frequency of the "the reference clock 200"; it is a "second device" (e.g., the "semiconductor chip 101a") of Umemura that performs the selection of the frequency of a signal for subsequent use.

"The semiconductor chip 101a includes a phase-locked loop (PLL) circuit 103a which is designed to receive a reference clock signal [200] from a source oscillator 100 to thereby output a predetermined frequency-multiplied clock signal, a predetermined frequency-divided clock signal and a polyphase clock signal, respectively, ... " (See Umemura, col. 15, lines 32-37).

The "select" capability of Umemura as not being in the first device or "source oscillator 100", but rather being in a second device, or one of the "semiconductor chips 101a, 101b and 101c" is perhaps even more clear as depicted below.

"Each of the semiconductor chips 101a, 101b and 101c is supplied with the system reference clock signal [200] from the source oscillator 100 to thereby allow the frequency-multiplied clock signal, the frequency-divided clock signal and the polyphase clock signal to be generated by the phase-locked loop circuits 103a, 103b and 103c, respectively, so that these clock signals are made available in the semiconductor chips 101a, 101b and 101c." (See Umemura, col. 17, lines 5-12).

As mentioned above, the Examiner asserts that the "first device" and the "second device" of the Applicant's claimed subject matter correspond to reference numerals 401 (first device) and 400 (second device) of Umemura; these element are a "first semiconductor chip 401" and a "second semiconductor chip 400" of the FIG. 10 of Umemura.

Clearly, the "oscillation unit" as described in the Examiner cited portions of Umemura (which the Examiner identifies as being equivalent to the Applicant's "clock generation circuitry") is not even located in the "first semiconductor chip 401" or in the "second semiconductor chip 400" of the FIG. 10 of Umemura.

Moreover, it is noted that within these Examiner identified elements of Umemura, it is not the "first semiconductor chip 401" (i.e., first device) that performs the selection

of the frequency of the clock signal, but rather the "second semiconductor chip 400" (i.e., second device) that performs the selection.

"In the synchronous data transfer system according to the second embodiment of the present invention, the second semiconductor chip 400 utilizes as the phase reference signal the loop-back clock signal RCLK sent from the address buffer 403 of the first semiconductor chip 401 and received via the loop-back clock bus 407. A control circuit 409 composed of an edge detection circuit, a clock select circuit, a change-over circuit for the clock select circuit and a clock change-over switch as incorporated in the second semiconductor chip 400 selects a clock signal from the phase reference signal mentioned above for latching the data from the data bus 406 which data are to undergo the synchronous transfer." (See Umemura, col. 24, lines 52-64, emphasis added).

Clearly, this clock select capability is included in the "second semiconductor chip 400" (i.e., second device) and not in the "first semiconductor chip 401" (i.e., first device).

"Besides, when the operation for reading the memory device 402 mounted on the first semiconductor chip 401 on which the address buffer 403 itself is mounted is detected, the clock of one cycle is derived from the clock signal CLK of the clock bus 405 to be outputted onto the loop-back clock bus 407." (See Umemura, col. 24, lines 8-13, emphasis added).

Clearly, the "first semiconductor chip 401" (i.e., first device) does not select the clock to be employed on the "clock bus 405" or on the "loop-back clock bus 407"; this is performed rather by the "second semiconductor chip 400" (i.e., second device). The "first semiconductor chip 401" (i.e., first device) does in fact process and make decisions using the "clock signal CLK of the clock bus 405", but the "first semiconductor chip 401" (i.e., first device) does not select the frequency or phase of either of the "clock signal CLK of the clock bus 405" or the clock signal "to be outputted onto the loop-back clock bus 407".

As mentioned above, in many locations of Umemura, the description of "plurality of nodes connected to said oscillation unit" or "a plurality of nodes connected to the oscillation circuit" is provided. Each of the nodes is described as including "at least an internal logic circuit". The "semiconductor chips 101a, 101b and 101c" include internal

logic circuits 105a and 105b" and "internal logic circuit 105c", and the "semiconductor chip 101d" includes "internal logic circuit 105d", respectively.

It may therefore properly be interpreted that the "semiconductor chips 101a, 101b and 101c" and the "semiconductor chip 101d" are in fact the "plurality of nodes" that are connected to "said oscillation unit" or "the oscillation circuit" according to Umemura. The "second semiconductor chip 400" (i.e., second device) of the FIG. 10 of Umemura also includes "internal logic circuit 105d".

It may therefore logically be inferred that the "second semiconductor chip 400" (i.e., second device) of the FIG. 10 is also connected to "said oscillation unit" or "the oscillation circuit" in similar fashion as the "semiconductor chips 101a, 101b and 101c" and the "semiconductor chip 101d".

Clearly then, although the "second semiconductor chip 400" (i.e., second device) of the FIG. 10 of Umemura does in fact include clock selection capability as described above, it does not include the "oscillation unit" or "oscillation circuit" (i.e., the "source oscillator 100" that provides the "reference clock signal 200"). Clearly, neither of the "first semiconductor chip 401" (i.e., first device) nor the "second semiconductor chip 400" (i.e., second device) of the Examiner cited portions of Umemura include any "clock generation circuitry" according to the subject matter as claimed by the Applicant.

In contradistinction, according to the Examiner cited portions of Umemura, it is the "oscillation unit" or "oscillation circuit" (i.e., the "source oscillator 100" that provides the "reference clock signal 200") that generates the clock signal that is used by the "plurality of nodes".

Therefore, the Applicant respectfully believes that the Examiner's cited portions of Umemura do not meet the limitations of the Applicant's claimed subject matter (except for the pin functionality for which the Examiner brings in Voit).

The Applicant respectfully asserts that the "first semiconductor chip 401" (i.e., first device) of Umemura is not a "first device [that] comprises a clock generation circuit (an oscillation unit for generating clock signal, col. 3, lines 40-45) for selecting and providing a clock signal to the second device". Since a clock signal is not generated within the "first semiconductor chip 401" (i.e., first device), but rather in the "oscillation unit" or "oscillation circuit" (i.e., the "source oscillator 100" that provides the "reference

clock signal 200") according to the Examiner cited portions of Umemura, it clearly may not be selected there from.

Moreover, the Examiner cited "clock signal" is not even generated by the "second semiconductor chip 400" (i.e., second device), but rather by the "oscillation unit" or "oscillation circuit" (i.e., the "source oscillator 100" that provides the "reference clock signal 200") to the "second semiconductor chip 400" (i.e., second device) that includes the "internal logic circuit 105d".

With respect to Voit, the Examiner states:

"Voit discloses a selection control pin (120) in a clock circuit (100) used to select at least one of the frequency of the clock signal and the phase of the clock signal (col. 4, line 54 to col. 5, line 10)." (see OA, Part of Paper No./Mail Date 20050427, p. 3).

The Applicant points out that FIG. 2 of Voit includes a "circuit 100 generally comprises a reference clock generator 102, a clock driver 104, at least one peripheral component interconnect (PCI) slot 106, a direct current voltage source 108, a resistor 110, and a bus controller 112." (See Voit, col. 4, lines 37-42, emphasis added).

It appears quite clear that the "reference clock generator 102" is the element of this circuit 100 that performs clock generation.

According to Voit, the "PLL 104 has two inputs 116, 118 for reference clock signals and a selection control pin 120 to select which of the two inputs 116, 118 is to be the basis of the output signals 122, 124." (See Voit, col. 4, lines 58-64).

The "selection control pin 120" is part of the "PLL 104", and not part of the "reference clock generator 102". Clearly, although the "PLL 104" does perform selection of "which of the two inputs 116, 118 is to be the basis of the output signals 122, 124", the "PLL 104" does not include any "clock generation circuitry" to generate the reference clock signals as they are inputs (i.e., "two inputs 116, 118") from which outputs (i.e., "output signals 122, 124") are selected.

According to the "circuit 100" of Voit, there is no first device that is capable to generate a clock signal as well as to comprise a pin that is used to select at least one of a frequency of the clock signal and a phase of the clock signal in accordance with the subject matter as claimed by the Applicant in claim 1. Two distinct devices (the "reference clock generator 102" and the "PLL 104" having the "selection control pin

120") are employed; one performs the actual clock generation and the other performs selection of the frequency.

According to the subject matter as claimed by the Applicant in claim 1, a "the first device comprises a clock generation circuitry, the clock generation circuitry being operable to select and to provide a clock signal to the second device, the clock signal having a frequency and a phase; and the first device further comprises a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device."

The Applicant respectfully asserts that the inclusion of Voit with Umemura fails to overcome the deficiencies of Umemura with respect to claim 1. The Applicant respectfully believes that claim 1 is allowable over Umemura in view of Voit.

The Applicant respectfully asserts that the combination of Umemura fails to teach each and every limitation of "An inter-device adaptable interfacing clock skewing system, comprising: a first device; and a second device that is communicatively coupled to the first device; and wherein the first device comprises a clock generation circuitry, the clock generation circuitry being operable to select and to provide a clock signal to the second device, the clock signal having a frequency and a phase; and the first device further comprises a pin that is used to select at least one of the frequency of the clock signal and the phase of the clock signal that is provided to the second device."

In view of the comments made above, the Applicant respectfully requests that the Examiner withdraw the rejection to claim 1 under 35 U.S.C. § 103(a) as being unpatentable over Umemura in view of Voit.

The Applicant respectfully believes that claim 6, being a further limitation of the subject matter of claim 1, is also allowable.

With respect to claim 2, the Examiner states:

"Regarding claim 2, Voit discloses the second device selecting the pin (a peripheral component interconnect (PCI) slot 106, see FIG. 2." (see OA, Part of Paper No./Mail Date 20050427, p. 4).

Under this rationale provided by the Examiner, the "PCI slot 106" would constitute the 2nd device and the 1st device would therefore be the "PLL 104" that includes the "selection control pin 120". The Applicant acknowledges that the "PCI slot

106" provides the "M66EN" signal to "control the output of the PLL 104 via the selection control pin 120". However, as mentioned above with respect to Voit, the "PLL 104 does not include clock generation circuitry", but rather the "reference clock generator 102" is operable to generate the clock signals from which the "PLL 104" selects. This interpretation of Voit also fails to meet all of the limitations of the Applicant's claimed subject matter.

The Applicant respectfully asserts that the inclusion of Voit with Umemura fails to overcome the deficiencies of Umemura with respect to claim 2. The Applicant respectfully believes that claim 2 is allowable over Umermura in view of Voit. The Applicant respectfully believes that claim 2, being a further limitation of the subject matter of claim 1, is also allowable.

With respect to claim 5, the Applicant respectfully points out that claim 5 depends on claim 3. Claim 3 further depends on claim 1. The Examiner has indicated that claim 3 is "objected to" (not rejected) as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The Applicant respectfully believes that claim 1 is allowable, and the Applicant respectfully believes that claim 5, being a further limitation of the subject matter of claim 3 (which itself depends on claim 1), is also allowable.

With respect to claim 11, the Examiner states:

"Regarding claim 11, Umemura et al disclose the first device comprising phase locked loop (PLL) operable to perform phase shifting of the clock signal before the clock signal is provided to the second device (col. 19, lines 52-63)." (see OA, Part of Paper No./Mail Date 20050427, p. 4).

As mentioned above, "The semiconductor chip 101a includes a phase-locked loop (PLL) circuit 103a which is designed to receive a reference clock signal [200] from a source oscillator 100 to thereby output a predetermined frequency-multiplied clock signal, a predetermined frequency-divided clock signal and a polyphase clock signal, respectively, ... " (See Umemura, col. 15, lines 32-37, emphasis added).

As also mentioned above, in accordance with the Examiner's interpretation of Umemura, the Examiner identifies "an oscillation unit for generating clock signal, col. 3, lines 40-45" (i.e., "said oscillation unit" or "the oscillation circuit" which is the "source

oscillator 100") as corresponding to the "first device" of the Applicant's claimed subject matter that includes the "clock generation circuitry". Clearly, the Examiner identified "first semiconductor chip 401" (i.e., first device) does not include this Examiner identified "said oscillation unit" or "the oscillation circuit" which is the "source oscillator 100" of Umemura.

Under this Examiner interpretation of Umemura, the "semiconductor chip 101a [that] includes a phase-locked loop (PLL) circuit 103a" of Umemura would constitute a "second device". Clearly, this does not meet the subject matter as claimed by the Applicant in claim 11.

The Applicant respectfully believes that claim 11 is allowable, and the Applicant respectfully believes that claim 11, being a further limitation of the subject matter of claim 1, is also allowable.

With respect to claim 14, the Examiner states:

"Regarding claim 14, Umemura et al disclose wherein the second device providing at least one additional clock signal to the first device (see Figure 10)." (see OA, Part of Paper No./Mail Date 20050427, p. 4).

While the Applicant acknowledges that the "second semiconductor chip 400" (i.e., second device) provides the "clock signal CLK of the clock bus 405" to the "first semiconductor chip 401" (i.e., first device), the Applicant respectfully points out that the combination of Umemura and Voit fails to meet the other limitations of the subject matter of claim 1, on which claim 14 depends. The "second semiconductor chip 400" (i.e., second device) and the "first semiconductor chip 401" (i.e., first device) are not the first device and the second device, respectively, of the subject matter as claimed in claim 1 by the Applicant.

Therefore, the Applicant respectfully believes that claim 14 is allowable, and the Applicant respectfully believes that claim 14, being a further limitation of the subject matter of claim 1, is also allowable.

With respect to claim 15, the Examiner states:

"Regarding claim 15, Umemura et al disclose wherein the second device providing data to the first device (see Figure 10)." (see OA, Part of Paper No./Mail Date 20050427, p. 4).

While the Applicant acknowledges that "transferred from the second semiconductor chip 400 to the memory device 402 via the data bus 406 is write data DATA". (See Umemura, col. 24, lines 37-39), which is the transfer of data from the "second semiconductor chip 400" (i.e., second device) to the "first semiconductor chip 401" (i.e., first device), the Applicant respectfully points out that the combination of Umemura and Voit fails to meet the other limitations of the subject matter of claim 1, on which claim 15 depends.

The "second semiconductor chip 400" (i.e., second device) and the "first semiconductor chip 401" (i.e., first device) are simply not the first device and the second device, respectively, of the subject matter as claimed by the Applicant in claim 1.

Therefore, the Applicant respectfully believes that claim 15 is allowable, and the Applicant respectfully believes that claim 15, being a further limitation of the subject matter of claim 1, is also allowable.

With respect to claim 32, the Examiner states:

"Regarding claim 32, Umemura et al disclose the phase difference comprising one zero and 90 degrees (col. 17, line 33-46)." (see OA, Part of Paper No./Mail Date 20050427, p. 5). This Examiner cited portion of Umemura is provide below.

"Under the conditions mentioned above, so long as the data as transferred can guarantee or secure sufficiently the data-effective time to be secured by the flip-flop circuits 104e and 104f, there exists internally of the semiconductor chip 101c the clock-signal which can be latched without fail. In the case of the synchronous data transfer system according to the first embodiment of the invention, each of the internal logic circuits 105a, 105b and 105c incorporated in the semiconductor chips 101a, 101b and 101c, respectively, operates basically with the zeroth phase φ0. However, the internal logic circuit 105a; 105b; 105c may equally be so implemented as to operate with polyphase such as two phases φ0 and φ3 or with three phases φ0, φ2 and φ4 or the like, when occasion requires, although illustration is omitted." (See Umemura, col. 17, lines 33-46, emphasis added).

While this portion of Umemura does identify a "zeroth phase", there is no mention of "ninety degrees." In addition, the Applicant respectfully points out that the

combination of Umemura and Voit fails to meet the other limitations of the subject matter of claim 31, on which claim 32 depends.

For most of the remaining claims, 16, 18, 19, 21, 22, 26, 29, 30, 31, 32, 33, 34, 39, 40, 41, 43, 44, 63, 64, 70-71, 73-74, the Examiner states that these claims are similar to previously rejected claims, and they are "rejected under a similar rationale."

The Applicant has dutifully tried to point out the patentability of claims 1-2, 5, 6, 11, 14, 15, 16 over Umemura in view of Voit.

As such, the comments made above are also applicable with respect to claims 16, 18, 19, 21, 22, 26, 29, 30, 31, 32, 33, 34, 39, 40, 41, 43, 44, 63, 64, 70-71, 73-74. The Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-2, 5, 6, 11, 14, 15, 16, 18, 19, 21, 22, 26, 29, 30, 31, 32, 33, 34, 39, 40, 41, 43, 44, 63, 64, 70-71, 73-74 under 35 U.S.C. § 103(a) as being unpatentable over Umemura in view of Voit.

Allowable Subject Matter

5. In the above-referenced OA, the Examiner has indicated that claims 45-50, 51-62, and 75-76 are allowed.

6. In the above-referenced OA, the Examiner has indicated that claims 3, 4, 7, 8, 9, 10, 12, 13, 17, 20, 23, 24, 25, 27, 28, 35, 36, 37, 38, 42, 65, 66, 67, 68, 69, 72 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In view of the comments made above with respect to the independent claims to which claims 3, 4, 7, 8, 9, 10, 12, 13, 17, 20, 23, 24, 25, 27, 28, 35, 36, 37, 38, 42, 65, 66, 67, 68, 69, 72 depend, either directly or interveningly, the Applicant respectfully requests that the objection to claims 3, 4, 7, 8, 9, 10, 12, 13, 17, 20, 23, 24, 25, 27, 28, 35, 36, 37, 38, 42, 65, 66, 67, 68, 69, 72 be withdrawn in view of the allowance of those corresponding independent claims.

The Applicant respectfully believes that claims 1-76 are in condition for allowance and respectfully requests that they be passed to allowance.

The Examiner is invited to contact the undersigned by telephone or facsimile if the Examiner believes that such a communication would advance the prosecution of the present patent application.

RESPECTFULLY SUBMITTED,

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